REMARKS

The above amendments and following remarks are submitted in response to the Office Action of the Examiner mailed March 7, 2005. Having addressed all objections and grounds of rejection, claims 1-20, being all the pending claims, are now deemed in condition for allowance. Entry of these amendments and reconsideration to that end is respectfully requested.

Even though most of the claims have been rejected on a new ground of rejection involving the application of newly cited prior art, the Examiner has kindly commented upon Applicants' previous arguments to the extent applicable to the new ground of rejection. Applicants wish to express their gratitude for this gesture by the Examiner which is deemed most helpful in understanding the differences which are still present within the respective positions of the Examiner and Applicants.

Claims 6-10 have been rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,330,630, issued to Bell (hereinafter referred to as "Bell"). In response thereto, claims 6-10 have been amended as suggested by the Examiner in his remarks on pages 6-7. Specifically, claim 6 has been amended to limit the claimed "multiplexing" to "switching" inputs and outputs of the claimed data busses. Though support for this added limitation is found throughout Applicants' disclosure, particular attention to

the subject is given in Fig. 7 and associated discussion at page 9 of the specification.

Clearly, the "switching" limitation distinguishes over Bell in that any suggestion in Bell to "combine" the two busses is without disclosure of any "switching" structural elements. The rejection of claim 6, as amended, and all claims depending therefrom, is respectfully traversed.

Applicants have previously made their arguments concerning the independent patentability of claims 7-10 which depend from claim 6. Because of the further limitations to claim 6 from which claims 7-10 depend, it is assumed that the Examiner will now find the claimed combinations therein independent patentable as has been previously argued.

Claims 1-5 and 11-20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Bell in view of US. Patent No. 5,881,294, issued to Downey et al (hereinafter referred to as "Downey"). In addition to the amendments made to claims 1, 11, and 16 consistent with the discussion of claim 6 above, the rejection of claims 1-5 and 11-20 is respectfully traversed for failure of the Examiner to present a *prima facie* case of obviousness as specified by MPEP 2143.

To present a *prima facie* case of obviousness in accordance with the requirements of MPEP 2143, the Examiner has the burden of presenting evidence and making arguments to show: 1)motivation to

make the alleged combination; 2)reasonable likelihood of success of the alleged combination; and 3)all claimed elements within the alleged combination. The Examiner has simply not met his burden of proof in regard to any of these three required showings.

With regard to "motivation", for example, the Examiner simply states:

> It would have been obvious to one of ordinary skill in the art to combine Downey with Bell, because Downey shows a means to respond to interrupts from multiple locations using a convenient centralized handling logic.

This statement has nothing to do with the requirement to show "motivation" because it does no present evidence or argument "why" one would be motivated to make the alleged combination. Therefore, the Examiner has failed to show motivation.

With regard to the obligation of the Examiner to address "reasonable likelihood of success", the record is silent. The Examiner has simply ignored this requirement.

The third required showing is that the alleged combination have all of the claimed elements. Downey has been cited and applied to meet the limitation of "a circuit having a single set of interrupt logic and a selector" which the Examiner admits is not found in Bell. In support of his rejection, the Examiner cites Fig. 6 and column 11, lines 38-45, of Downey. However, Downey does not have this element

either. Though arguably Downey routes interrupts through a common circuit, that circuit does not have any data bus selection capability. Furthermore, Programmable Interrupt Router 607 cannot simply be added to Bell, because of the need to handle both data and control signals over the claimed busses.

As a result, the Examiner has not made any of the three showings required by MPEP 2143 to present a *prima facie* case of obviousness. Furthermore, it is clear that the Examiner has continued his misrepresentation of the claimed invention with regard to a number of dependent claims. For example, in rejecting claims 5, 15, and 20, the Examiner states that "Bell also discloses the rate is 33 MHz (e.g., col. 5, line 9)". Whereas the statement is true, it is irrelevant, because claims 5, 15, and 20 are limited by a **66 MHz** maximum rate.

Thus, the rejection of claims 1-5 and 11-20 are respectfully traversed for failure of the Examiner to make any of the three showings required by MPEP 2143 to present a *prima facie* case of obviousness.

Having thus responded to each objection and ground of rejection, Applicants respectfully request entry of this amendment and allowance of claims 1-20, as amended, being the only pending claims.

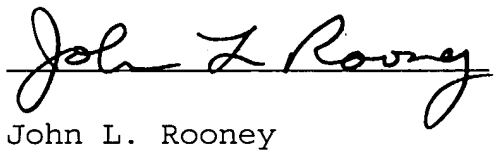
Please charge any deficiencies or credit any overpayment to Deposit Account No. 14-0620.

Respectfully submitted,

Lloyd E. Thorsbakken et al.

By their attorney,

Date June 7, 2005



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